MONOLITHIC V-BAND PSEUDOMORPHIC-MODFET LOW-NOISE AMPLIFIERS*

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ABSTRACT

V-band, low-noise MMICs based on pseudomorphic modulation-doped FETs (P-MODFETs) have been developed for the first time and have yielded noise figures that are believed to be the lowest reported for any millimeter-wave MMIC. Single-stage low-noise amplifiers with P-MODFETs as active elements (gate dimensions 0.35 x 60 μm) exhibited minimum noise figures of 3.9 dB at 58 GHz, with an associated gain of 3.5 dB. Dual-stage MMICs had minimum noise figures of 5.3 dB at 58 GHz, with an associated gain of 8.2 dB, and maximum gain of 10.4 dB at 59.5 GHz. Further, a cascaded four-stage amplifier (two dual-stage MMIC modules) exhibited a 5.8-dB minimum noise figure at 58 GHz, with an associated gain of 18.3 dB, and 21.1 dB of maximum gain. Device processing uniformity, as well as DC and RF reliability data, are also presented.

INTRODUCTION

Monolithic millimeter-wave integrated circuits are expected to have potential application in missle seekers, intersatellite links, and phased-array radar syastems. Thus far, these circuits have been primarily based on GaAs metal-semiconductor FET (MESFET) technology [1],[2]; however, such technology has performance limitations for millimeter-wave applications. Recently, a relatively new technology has emerged which promises greater performance advantages than MESFET-based MMICs. These millimeter-wave monolithic circuits use standard GaAs/AlGaAs modulation-doped FET (MODFET) or pseudomorphic InGaAs/GaAs MODFET (P-MODFET) structures as the active component(s). MODFET-based, single-stage low-noise amplifiers (LNAs) and three-stage monolithic Q-band amplifiers have been reported at 42 to 47 GHz [3],[4].

This paper reports, for the first time, on the use of strained-lattice-matched MODFET structures of InGaAs-on-GaAs substrates for V-band MMICs. These structures are called "pseudomorphic" MODFETs because the thin InGaAs layer deforms during epitaxial growth to match the lattice constant of GaAs. Because the P-MODFET offers better electron confinement within the FET channel, as well as higher saturated electron velocities than either GaAs MESFETs or GaAs/AlGaAs MODFETs, most RF figures of merit, such as noise figure and gain, can be substantially improved by using P-MODFETs as the active component in MMICs. Further, because the starting substrate material is still GaAs (rather than InP, for example), all of the processing techniques developed for conventional GaAs MODFETs continue to be applicable. Although $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As/InP$ MODFETs have shown improved performance compared to P-MODFETs, controlling the indium mole fraction to 1 percent or better to ensure a lattice-matched device structure is difficult. The RF and DC results presented here clearly illustrate the high-performance capabilities, reliability, and reproducibility that can be achieved by using P-MODFETs in millimeter-wave MMICs.

DEVICE AND CIRCUIT DESIGN

Figure 1 shows the P-MODFET structure used to fabricate the V-band LNAs in this study. This structure was developed empirically, and discrete 0.30 x 60-μm devices were fabricated and tested at 14 GHz to evaluate their potential for V-band MMIC LNA applications. These P-MODFET devices have produced low noise figures of approximately 0.9 dB, with associated gains of about 12 dB. Using the Fukui equation as an approximate model, the design of the device structure was adjusted to optimize several DC parameters (e.g., g_m, C_{gs}, R_s, and R_g). However, a theoretical model was recently implemented that incorporates both classical and quantum mechanical calculations to determine the channel sheet charge density, which can then be used to calculate device parasitics and I-V characteristics. These calculations indicate that, while the device structure mentioned previously is suitable for high performance, a number of structural/material changes could be made to further reduce the noise figure.

Since the accuracy of most MESFET circuit models above 30 GHz is questionable, and since the equivalent circuit parameters for the P-MODFET are not too different from those for the MESFET, an existing V-band MESFET LNA maskset [2] was selected for the first iteration. However, to accommodate some deviations from the original MESFET design, tuning islands were incorporated into the circuit layout which could then

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be connected via direct e-beam writing. This approach allowed slight adjustments to the matching circuit without additional mask fabrication. The dual-stage amplifier design (Figure 2) uses a via-hole, source-grounded P-MODFET and an interstage distributed matching network to obtain low noise, gain flatness, and good return loss performance across the frequency band. A transmission line model of the input and output DC-blocking capacitors was used to account for their distributive characteristics. Input and output biases were provided by the shunt RF-shorted elements, which were grounded through metal-insulator-metal (MIM) capacitors and via-holes.

EPITAXIAL GROWTH AND MMIC FABRICATION

The P-MODFET structures were grown in a RIBER 2300 molecular beam epitaxy (MBE) system. The growth and preparation conditions for these structures were similar to those documented elsewhere [5],[6]. Substrate temperatures were continuously varied between 510°C (for the InGaAs layer) and 590°C (for the AlGaAs layer).

Since the growth of the lattice-strained InGaAs-to-GaAs substrate requires careful determination of both the InGaAs channel thickness and the indium concentration, it is recommended that in situ reflection electron diffraction (RED) oscillations be monitored to accurately determine growth rate and thickness. Because InGaAs does not have the same lattice constant (atomic spacing) as GaAs, there is a fundamental limit (for any given indium concentration) [7] on the InGaAs film thickness before dislocations form in the material and ultimately affect device performance. However, below this thickness limit the P-MODFET devices presented here have exhibited DC stability as good as or better than that of the GaAs MESFETs. This point will be discussed in a later section. Nevertheless, it should be emphasized that all the structures used in this study were grown below the thickness limit.

Chip fabrication begins with the etching of mesas (~2,000 to 3,000 Å in height) in the MBE-grown film to provide device isolation ($R > 10^7$ Ω). A Au/Ge/Ni/Ag/Au alloy is then produced by rapid thermal anneal to form the ohmic contacts ($R_c \leq 0.1$ Ω-mm). Next, direct-write e-beam lithography (Cambridge EBMF 10.5 system) is used to define the submicron-length gates (~0.35 μm), as well as to connect the tuning elements for a better match with the device impedance.

The source-to-drain channel current is monitored during gate recess etching to determine the desired etch depth. Because most P-MODFET structures are very thin (channel-to-surface height) relative to the MESFET, the gate recess is often quite shallow. Consequently, very good device uniformity can be obtained.

Figure 3 is a histogram of I_{dss} for 60 of the 0.35 x 60-μm devices. As can be seen, the variation in I_{dss} ($I_{dss} \propto$ doping-thickness product) over a 2-in. substrate is only about 13 percent. This variation in I_{dss} and V_p is typical of the 0.35-μm gate length MODFET process. It was found empirically that this gate size and geometry result in very few gate-related failures (<10 percent). Further, the gate length variation ($3\sigma/L_g$ percent), as measured on approximately 600 devices in the Cambridge system, is about 21 percent for the 0.25-μm gate length devices and about 10 percent for the 0.35-μm device wafer. Clearly, selection of the 0.35-μm geometry is a compromise between amplifier performance and circuit operating uniformity (bias uniformity, etc.).

The Si_3N_4 dielectric for the MIM capacitor (~2,500 Å) and device passivation (~1,500 Å) was deposited by plasma-enhanced chemical vapor deposition (PECVD), with an index of refraction of approximately 1.98. Air-bridges, capacitor top plates, and transmission lines were fabricated using two mask levels. Through-substrate via-holes were obtained by infrared alignment and spray etch techniques to provide low-inductance grounding for the P-MODFET sources and the shorted shunt elements. The chip size for the dual-stage LNA MMIC is 2 x 0.75 x 0.08 mm. Figure 2 shows the completed two-stage P-MODFET LNA MMIC.

DEVICE AND AMPLIFIER CHARACTERISTICS

Table 1 presents the normalized DC and RF equivalent circuit elements for a discrete P-MODFET, as determined from S-parameter measurements under high-gain bias. The MODFET lumped-element equivalent circuit is depicted in Figure 4. One distinguishing characteristic of P-MODFETs is their very high extrinsic transconductance values (g_m > 500 mS/mm). Typically, this transconductance is about a factor of 2 times higher than in conventional GaAs MESFETs with the same geometry. Figure 5 is a histogram of extrinsic g_m, as measured on 60 discrete devices across a 2-in. wafer ($g_m \propto 1/d$, where d is the distance between the gate metal and 2DEG). In this case, variations of only 6 percent were obtained. Figures 3 and 5 indicate the reproducibility of this growth and fabrication process, which leads to the high degree of DC uniformity obtained in these P-MODFET structures.

Table 1. Normalized DC and RF P-MODFET Parameters

Parameter	DC Measurement	S-Parameter Measurement
g_m, Extrinsic	500 mS/mm	--
g_m, Intrinsic	1,000 mS/mm	913 mS/mm
R_s	0.45 Ω-mm	0.15 Ω-mm
R_g	1.1 Ω-mm	0.56 Ω-mm
R_d	0.4 Ω-mm	0.26 Ω-mm
R_i	--	0.51 Ω-mm
G_o (or G_{DS})	18.8 mS/mm	20.0 mS/mm
C_{gs}	--	2.6 pF/mm
C_{dg}	--	0.25 pF/mm
C_{ds}	--	0.03 pF/mm
C_{dc}	--	0.05 pF/mm

The waveguide-to-microstrip transitions used previously for V-band MESFET LNAs [2],[8] were also used in the present work. The measured insertion and return losses shown in Figure 6 for one waveguide-to-microstrip transition were 0.5 dB and better than 18 dB, respectively, from 50 to 60 GHz. The MMICs were mounted on a metal test fixture (Figure 7), which included bias feedthroughs. This test fixture and MMIC design allowed ease of assembly and disassembly, and enabled modules to be cascaded in a multistage amplifier configuration. The RF loss of the 50-Ω transmission line was included in the measured results. A Hewlett-Packard 40- to 60-GHz measurement setup was used to obtain the frequency response. The noise figure was measured using a solid-state noise diode (calibrated from 55 to 65 GHz) and a Hewlett-Packard noise-figure meter [8].

Figure 8 shows the measured performance, under low-noise bias conditions, of a monolithic single-stage P-MODFET LNA from 56 to 60 GHz. A minimum noise figure of 3.9 dB, with an associated gain of 3.5 dB, was obtained for the single-stage MMIC at 58 GHz. Figure 9 depicts the noise figure and gain of a two-stage P-MODFET LNA MMIC from 56 to 60 GHz (at low-noise bias, V_g = +0.02 V and V_{ds} = 2.1 V). A minimum noise figure of 5.3 dB, with an associated gain of 8.2 dB, was obtained for the two-stage LNA MMIC, also at 58 GHz. A maximum gain of 10.4 dB was obtained at 59.5 GHz. In addition, a power density of 0.12 W/mm was achieved for this two-stage LNA at the 1-dB gain compression point (Figure 10). Nominally, from chip to chip and wafer to wafer, the low-noise bias conditions for the P-MODFET LNAs ranged from 2- to 3-V drain voltage, with -0.1 to +0.1 V gate bias.

To achieve usable gain for system applications, two MMIC modules (dual-stage) were cascaded. A four-stage amplifier exhibited a minimum noise figure of 5.8 dB, with an associated gain of 18.3 dB (at 58 GHz). A maximum gain of 21.1 dB was also obtained. Calculations based on the noise figure and gain from the single-stage LNA showed that noise figures of 4.9 dB (5.3 dB, measured) and 5.5 dB (5.8 dB, measured) cound be expected for the two-stage and cascaded four-stage LNAs, respectively. This small difference between the predicted and measured multistage LNA performance occurs in part because the performance of each stage cannot be optimized independently (i.e., each stage cannot be biased separately). Nevertheless, a comparison of the noise figures for the single-stage, two-stage, and cascaded four-stage MMICs emphasizes the importance of a uniform, high-yield fabrication process.

P-MODFET RELIABILITY

A number of experiments were conducted to assess the long-term reliability of the P-MODFETs under thermally stressed conditions. Approximately 30 discrete devices were passivated and then DC-characterized (i.e., g_m, I_{dss}, V_p, and V_{br}) to establish the initial device condition. These devices were then subjected to the following static (no bias) heat cycling sequence: start at 175°C, bake for 48 hours, and then DC-test; then continue up to and including 300°C for 48 hours in increments of 25°C, with complete DC-characterization after each increment. As a starting point, a measured variation of ≥20 percent in any of the above device parameters was arbitrarily established as a device failure criterion.

After the first bake (at 175°C), only one failure was recorded. At 200°C, one more failure was registered. At 225°C, no failures were recorded (and so forth). Three more devices were lost during the remainder of the heat cycling tests, including the last test at 300°C. In short, only 15 percent of the devices DC-failed after heat treatment at temperatures as high as 300°C, which far exceeds any normal channel temperature for a low-noise device, as well as for most power devices. Assuming an activation energy (from the literature) of 1.5 eV and a nominal channel temperature of 110°C, calculations indicate a mean time to failure of 1.3×10^9 hours! More realistically, a mean temperature to failure (i.e., half the devices would fail after 48 hours with this channel temperature) of 340°C was calculated, which is far superior to that for MESFETs. This calculation requires no assumptions regarding activation energy.

In addition, discrete devices of varying gate widths (60, 100, and 150 μm) which had undergone the heat cycling described above were measured for noise figure and gain at 14 GHz. They were then compared with devices from the same wafer (with the same gate width) that had not undergone the heat treatment. Of the eight devices tested (four unheated and four heated), virtually no change (i.e., ≤0.2 dB) was observed in either the noise figure or gain between the two lots. Although these RF data constitute only a small statistical sampling, there is every indication that P-MODFET-based MMICs represent a highly reliable technology.

CONCLUSIONS

Monolithic single-stage, dual-stage, and cascaded four-stage P-MODFET LNA MMICs have been designed and operated at V-band frequencies with minimum noise figures of 3.9, 5.3, and 5.8 dB, respectively (at 58 GHz). Associated gains from these amplifiers were 3.5, 8.2, and 18.3 dB, respectively. It is believed that these are the first reported results for any P-MODFET-based MMIC, and that the minimum noise figure of 3.9 dB obtained for the single-stage LNA is the lowest reported for any millimeter-wave MMIC.

These MODFET LNAs have the potential to operate at still higher frequencies, and certainly (with reduced gate length and/or T-shaped gates) their performance could be improved substantially. Additional changes to the LNA maskset to improve the input and output impedance-matching network are expected to further extend the usable frequencies of operation.

DC and preliminary RF data have also been presented which address the important issue of reliability for these strained-lattice structures. The data clearly indicate that the reliability of P-MODFET-based LNAs or power MMICs should be as good as or better than that of MMICs based on MESFET technology. With the proper device structure, good fabrication techniques, and good passivation, long-term reliability under extreme thermal loading does not appear to present any limitations to the P-MODFET.

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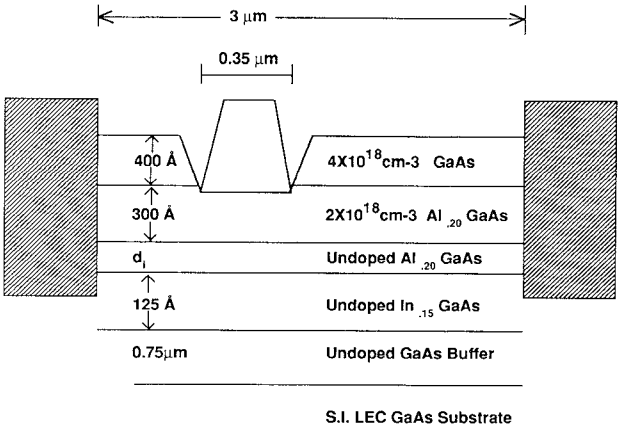

Figure 1. Cross-Sectional Schematic of the P-MODFET Structure

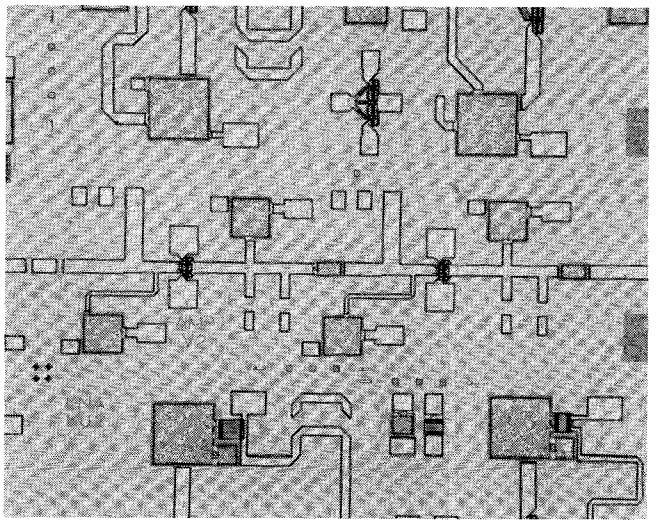

Figure 2. Monolithic V-Band Two-Stage P-MODFET LNA

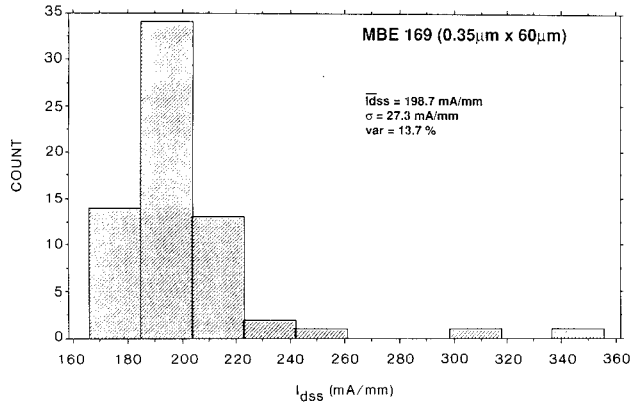

Figure 3. Histogram of Normalized I_{dss} Measured on 60 P-MODFETs Over a 2-in. Wafer

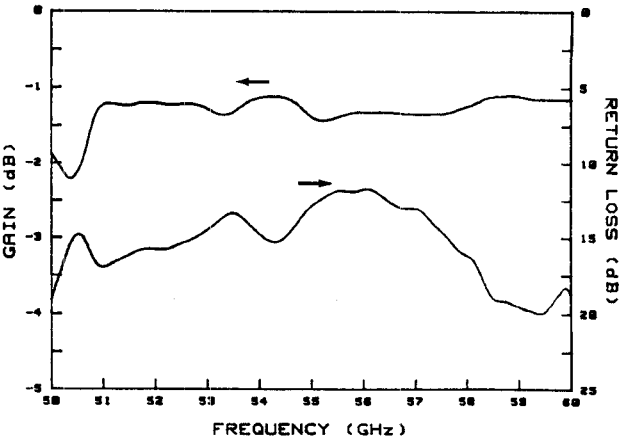

Figure 6. Performance of Two V-Band Waveguide-to-Microstrip Transitions

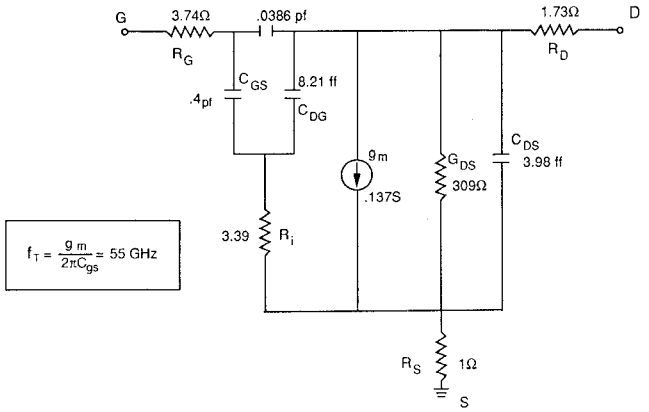

Figure 4. MODFET Lumped-Element Equivalent Circuit

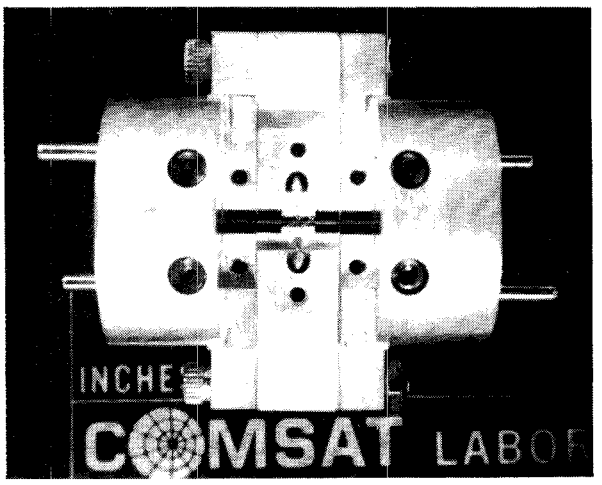

Figure 7. V-Band Fixture

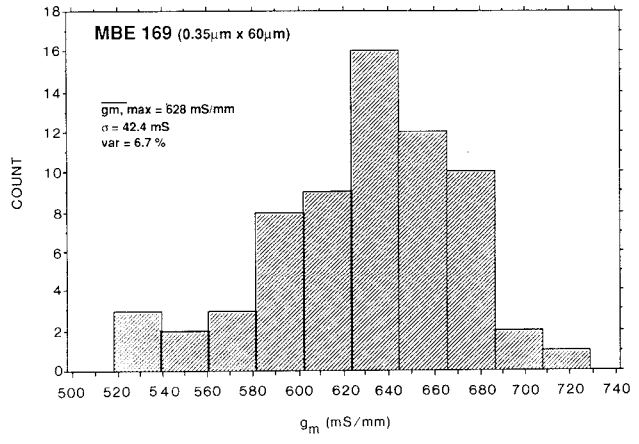

Figure 5. Histogram of Normalized Extrinsic Transconductance Over 60 Discrete P-MODFETs

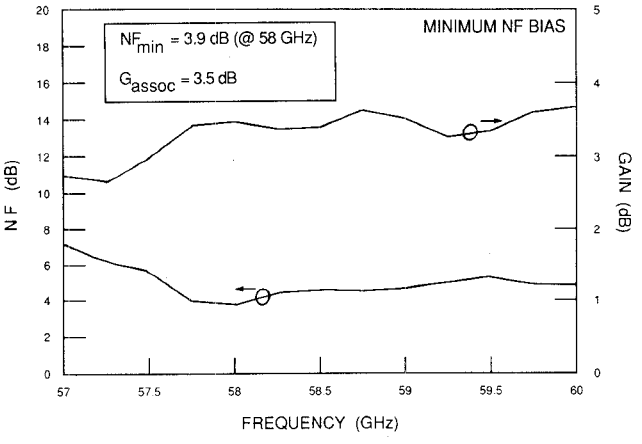

Figure 8. V-Band Single-Stage P-MODFET LNA MMIC RF Results

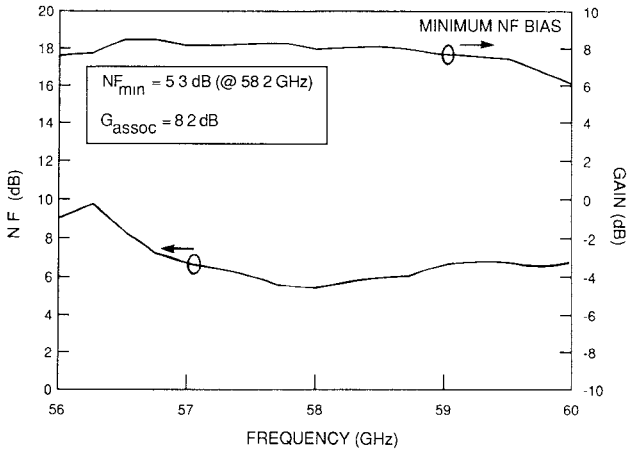

Figure 9. Two-Stage P-MODFET LNA RF Results: Low-Noise Bias

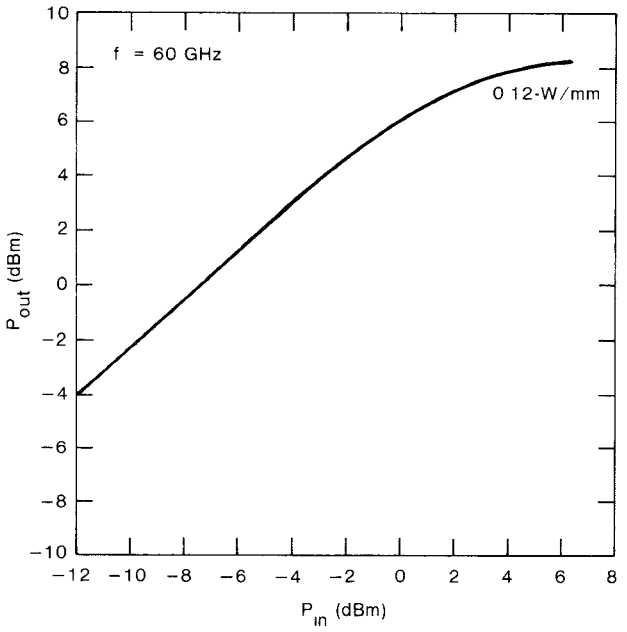

Figure 10. P_{out} vs P_{in} of a Two-Stage P-MODFET MMIC LNA